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# Design And Performance Analysis of Energy-Efficient Approximate Multipliers For Image Processing

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**ABSTRACT:** The goal of this paper is to create two new multipliers, each with an approximate size of 88, using compressors with a ratio of roughly 3:2 and 2:2. The multipliers generated from the Wallace multiplier design are equivalent to the "approximate Wallace multiplier" (AWM) discussed herein. The suggested AWMs were assessed and quantified using many "Design Metrics" (DMs), including area, power, delay, and the "power-delay-product" (PDP). Additionally, six distinct multipliers derived from the reported 3:2 compressors have been employed to evaluate AWM efficiency. Subsequent to the Verilog design, Cadence's "RTL Compiler" (RC) tool was employed to develop a 180 nm-optimized standard cell library for the fabrication of each multiplier. The proposed AWMs demonstrate high efficacy when utilized in conjunction with DMs, as indicated by the findings of the combination analysis. Image processing algorithms utilizing the previously stated approximation compressors compared the PSNR of AWMs with other Wallace multipliers. Upon comparison, it was determined that the proposed multipliers had a PSNR exceeding 50 dB.

***Keywords:*** *Approximate Computation, Wallace Multiplier, 3:2 Compressor, Low Power, PDP*

## 1. INTRODUCTION

Multimedia applications, including those managing audio, video, images, and voice, will impose a significant computational strain on the forthcoming generation of embedded systems. These application cases are remarkable since they adeptly manage a significant volume of computational errors when they arise. The aforementioned scenarios can be implemented with hardware that is imperfect or lacks precision. The efficiency and minimal precision requirements of suitable computing render it the favored approach over precise calculation in numerous instances. Digital Signal Processing (DSP) modules constitute the majority of the mathematical frameworks employed by multimedia applications, which perform a wide array of mathematical operations. The primary mathematical operations executed by these digital signal processor components are addition and multiplication. The adder circuit, a crucial component of the tested system, significantly impacts its utility and accuracy. Consequently, exploring methods to enhance the design and energy efficiency of digital signal processing (DSP) multiplier and adder circuits is perpetually intriguing.

Multimedia approximate multipliers have been extensively researched and discussed in recent years. We employ a 64-tap low-pass finite impulse response (FIR) filter to evaluate the efficacy of a Baugh-Wooley multiplier model. The text provides an expected multiplier for both signed and unsigned multiplication based on rounding. We compare and evaluate Dadda


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multipliers with Wallace trees for area, power, latency, and PDP. We assessed the four novel unsigned approximation multipliers, which utilize 4:2 compressors, based on power, latency, transistor count, and peak signal-to-noise ratio (PSNR). A significant quantity of 4:2 ratio compressors has been recently launched. This article examines an approximation multiplier derived from a modified 4:2 compressor. A multitude of multipliers has been examined and developed utilizing approximation mathematical circuits. A variety of full adder (FA) cells, each incorporating one or two more bits, were examined and analyzed at various theoretical levels.

The subsequent section presents a summary of the article's principal arguments. Section 2 offers an in-depth analysis of the distinctive approximation compressors and the proposed AWM. The final section examines the synthesis environment, analyzes the results from the simulations, and discusses potential image processing applications of the proposed multipliers. This is the fourth and final installment of the narrative.

## 2. DESIGN OF PROPOSED WALLACE MULTIPLIER USING NOVEL APPROXIMATE COMPRESSORS

This section examines the proposed 3:2 and 2:2 compressors and their implementation in the creation of an 88 AWM.

### PROPOSED COMPRESSORS

The article presents three innovative "approximate compressors" (ACs) labeled AC1, AC2, and AC3. AC1 and AC2 exhibit a 3:2 ratio, whereas AC3 and AC4 have a 2:2 ratio. To fabricate these compressors, we modify the "truth table" (TT) of the "exact compressors" (ECs), namely EC1 and EC2, which are accurate 3:2 and 2:2 compressors, respectively.

Table.1. A comparison of precise and approximate 3:1 blowers

| Inputs | | | $EC_1$ | | $AC_1$ | | $AC_2$ | |
|---|---|---|---|---|---|---|---|---|
| *A* | *B* | $C_{in}$ | *Sum* | $C_{out}$ | $Sum_1$ | $C_{out1}$ | $Sum_2$ | $C_{out2}$ |
| 0 | 0 | 0 | 0 | 0 | 1× | 0✓ | 1× | 0✓ |
| 0 | 0 | 1 | 1 | 0 | 1✓ | 0✓ | 1✓ | 0✓ |
| 0 | 1 | 0 | 1 | 0 | 0× | 0✓ | 0× | 0✓ |
| 0 | 1 | 1 | 0 | 1 | 0✓ | 0× | 0✓ | 0× |
| 1 | 0 | 0 | 1 | 0 | 0× | 1× | 0× | 0✓ |
| 1 | 0 | 1 | 0 | 1 | 0✓ | 1✓ | 0✓ | 0× |
| 1 | 1 | 0 | 0 | 1 | 0✓ | 1✓ | 0✓ | 1✓ |
| 1 | 1 | 1 | 1 | 1 | 0× | 1✓ | 0× | 1✓ |
| *ED* | | | - | | 4 | 2 | 4 | 2 |

Table.2. Examining the recommended and actual tables for a 2:2 compressor

| Inputs | | $EC_2$ | | $AC_3$ | |
|---|---|---|---|---|---|
| *X* | *Y* | *Sum* | $C_{out}$ | *Sum* | $C_{out3}$ |
| 0 | 0 | 0 | 0 | 1× | 0✓ |
| 0 | 1 | 1 | 0 | 1✓ | 0✓ |
| 1 | 0 | 1 | 0 | 1✓ | 0✓ |
| 1 | 1 | 0 | 1 | 0✓ | 1✓ |
| *ED* | | - | | 1 | 0 |

Table.3. Logic expressions for future AC output

| Proposed Compressor | Output Equations | |
|---|---|---|
| | *Sum* | $C_{out}$ |
| $AC_1$ | $\overline{A}+\overline{B}$ | $A$ |
| $AC_2$ | $\overline{A}+\overline{B}$ | $A{\cdot}B$ |
| $AC_3$ | $\overline{A}+\overline{B}$ | $A{\cdot}B$ |

Table 1 presents the AC TT. Table 2 presents the TT of ECs. The elements A, B, and C are included in the set. The three potential outcomes are Cout, Sum, and Cout2. All three "Sum" outputs are generated by the components of EC1, AC1, and AC2. They may be referred to as Sum, Sum1, and Sum2. Cour, Cout1, and Cout2 denote the "Carry" outputs on EC1, AC1, and AC2, respectively. Table 2 illustrates that X and Y correspond to the "Sum" values of EC2 and AC3, respectively. Sum, Cout, Sum3, and Cout3 represent the four possible outcomes.


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Similar to AC3, its "Carry" output is Cout, whereas EC2's is Cout3.

The truth tables of each alternating current are computed using the anticipated outputs and the accurate quantity of min-terms. We select the total quantity of min-terms and their placements to ensure that the logic equations for a certain approximation output conform to the stipulated requirements below. A method to adjust the "error distance" (ED) should exist. In the simplified output equation, the summation of products should not be depicted by several components. An excessive number of literals per line is prohibited in the SOP.

Initially, we must ascertain the numerical disparity between the estimated and actual data to compute the ED. Table 3 contains the logic diagrams corresponding to the simplified output equations for both the old and new compressors.

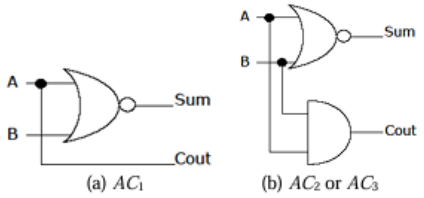



Fig.1. A preliminary sketch of the data flow diagram proposed for a compression method.

## DESIGN OF APPROXIMATE WALLACE MULTIPLIER

The document discusses the techniques for constructing an NM "approximate Wallace multiplier" (AWM) utilizing the proposed "approximate compressors" (ACs). M denotes the multiplier size, while N represents the multiplicand size. In this inquiry, eight-bit numbers are designated as N and M. The Wallace multiplier for exact compressors (ECs) comprises three components. The matter at hand involves three specific types of addition: carry-propagated addition (CPA), partial-product generation (PPG), and partial-product compression (PPC).

The PPG block generates 88 "partial products" (PPs), totaling 64. They create a grid measuring 8 by 15. The PPC block partitions the eight-row PP array into two-row segments to accommodate the final binary addition. The diminution of PP is executed in stages utilizing compressors.

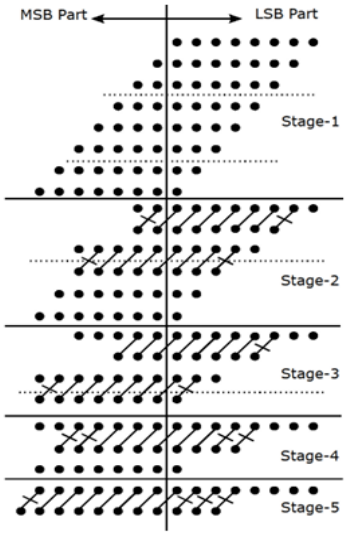



Fig.2. A gadget that reduces the power of an 8x8 Wallace multiplier.

The amalgamation of the two rows of PPs yields the final outcome. Figure 2 illustrates that a 3:1 compressor diminishes PP more efficiently than a 2:2 compressor. Two AWMs have been developed and evaluated to assess the efficacy of the proposed ACs. The AWM, developed using AC1 and AC3, is designated as "Proposed AWM1" (PAWM1). This AWM was built using AC2 and AC3 and is referred to as "Proposed AWM2" (PAWM2). The reduction circuits depicted in Figure 2 constituted the foundation for PAWM1 and PAWM2. The "Least Significant Bits" (LSB) and the "Most Significant Bits" (MSB) constitute this decimal numeral. Utilization of 3:2 and 2:2 compressors is standard before and after Stage 5 of LSB row addition, as well as during Stages 1 to 4 of PP reduction. In the


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MSB segment, the compressors are identical. AC1 and AC3 in PAWM1 utilize the LSB sector, while AC2 and AC3 in PAWM2 employ the same sector.

## 3.SIMULATION RESULTS AND DISCUSSION

The experimental outcomes are analyzed and compared to the proposed multipliers here. A collection of AWMs has been created and implemented for the purposes of research and evaluation. The developers of these systems refer to them as "Designed AWMs" (DAWMs). In the figure, reduction circuits were employed to ensure the functionality of all DAWMs.Reported compressors (RCs) offer an initial characterization of the compressor spectrum required for DAWMs. The logical equations derived from the truth table were employed for the production of all RCs. Table 4 presents the logical formulas employed to delineate the RC outputs.

Table.4. Statements for the Logic of Reported ACs (RCs) Output

| RC | Output Equations | | Ref. |
|---|---|---|---|
| | *Sum* | $C_{out}$ | |
| $RC_1$ | $A \oplus B \oplus C_{in}$ | $C_{in}$ | [12] |
| $RC_2$ | $A \oplus B$ | $A \cdot B$ | [12] |
| $RC_3$ | $\bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C}_{in} + \bar{B}\bar{C}_{in}$ | $A \cdot B + A \cdot C_{in} + B \cdot C_{in}$ | [12] |
| $RC_4$ | $\bar{C}_{in} \cdot \bar{A} \oplus \bar{B}$ | $B + A \cdot C_{in}$ | [15] |
| $RC_5$ | $\bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C}_{in}$ | $B + A \cdot C_{in}$ | [15] |
| $RC_6$ | $\bar{A} \cdot C_{in} + B \cdot C_{in}$ | $A$ | [15] |

Table.5. Mathematical formulas for the Precise Compressor EC

| EC | Output Equations | |
|---|---|---|
| | *Sum* | $C_{out}$ |
| $EC_1$ | $A \oplus B \oplus C_{in}$ | $A \cdot B + A \cdot C_{in} + B \cdot C_{in}$ |
| $EC_2$ | $A \oplus B$ | $A \cdot B$ |

The "exact Wallace Multiplier" (EWM) has been evaluated and proven to be effective. The EC1 and EC2 compressors were employed for the creation of EWM's LSB and MSB. Table 5 delineates the logical ideas employed in the development of these specific compressors. Initially, we juxtapose the EWM and DAWM against the power, delay, PDP, and area DMs calculated using the specified multipliers (PAWM1 and PAWM2).

**SYNTHESIS ENVIRONMENT**

Multipliers constructed using Verilog RTL instructions produced all of these DMs. The potential multipliers are validated using the Verilog test bench code generated by Cadence's "NCSim" tool. Furthermore, every potential multiplier was assessed with conventional Verilog test bench code. This is succeeded by employing the Cadence "RTL Compiler" (RC) to produce RTL codes that operate under the designated "Process-Voltage-Temperature" (PVT) conditions.

Figure 3 illustrates a procedure for extracting DMs from their native environment. The operation of the creation tool necessitates Verilog RTL code and the TSMC standard cell library for 180 nm technology. Upon receipt of these, Cadence's RTL translator (RC) generates a gate-level netlist that facilitates the identification of the necessary DMs. To facilitate an equitable comparison, each multiplier was delineated using Verilog RTL codes and synthesized at a supply voltage of 1.8V and a temperature of 27°C.

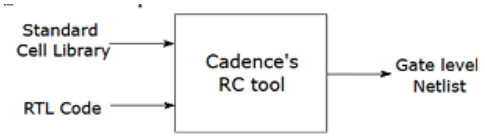



Fig.3. The degree of synthesis needed to obtain DMs

To enhance DM extraction post-synthesis, the input-drive strength and output-load parameters were modified. Our synthesis results are compared in a table with the performance of nearly developed and


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proposed Wallace multipliers about DMs.

| Approximate Multiplier | Power (nW) | | | Delay (ps) | PDP (fJ) | Area (μm²) |
|---|---|---|---|---|---|---|
| | Leakage | Dynamic | Total | | | |
| EWM | 31.978 | 505595.093 | 505627.071 | 6275 | 3172.80 | 4746.773 |
| DAWM1 | 26.814 | 482868.649 | 482895.463 | 5168 | 2495.60 | 4194.590 |
| DAWM2 | 30.460 | 459866.829 | 459897.289 | 5081 | 2336.73 | 4613.717 |
| DAWM3 | 22.727 | 368506.408 | 368529.135 | 5081 | 1872.49 | 3915.173 |
| DAWM4 | 28.364 | 389600.886 | 389629.249 | 5081 | 1979.70 | 4404.154 |
| DAWM5 | 20.948 | 359891.180 | 359912.129 | 5081 | 1828.71 | 3565.901 |
| DAWM6 | 21.186 | 338063.774 | 338084.960 | 5081 | 1717.81 | 3705.610 |
| PAWM1 | 18.857 | 300213.272 | 300232.129 | 5081 | 1525.48 | 2990.434 |
| PAWM2 | 21.087 | 294411.904 | 294432.991 | 5081 | 1496.01 | 3386.275 |

Two proposed multipliers, PAWM1 and PAWM2, possess total powers of 300.21 W and 294.41 W, respectively, as indicated in the "Power" column. Upon aggregating all the multipliers utilized for comparison, the recommended ones exhibit the least power. The proposed compressors consume less electricity due to their fundamental design.

Analysis of the 'Delay' column reveals that all proposed multipliers exhibited identical delays. The delay endures for 5.081 nanoseconds. Furthermore, DAWM2, DAWM3, DAWM4, DAWM5, and DAWM6 exhibit latency that is less than or equal to the prescribed multipliers.

The PDP column indicates that the PAWM1 has a PDP of 1525.5 fJ, whereas the PAWM2 has a PDP of 1496.01 fJ. Despite the existence of different multipliers, these PDP figures are the least substantial. The proposed multipliers exhibit the lowest Power Delivery Performance (PDP) due to their reduced power consumption and delayed reaction time.

Relative to alternative compressor designs, PAWM1 and PAWM2 occupy less space, as seen in the area column. One measures 2990.43 m², and the other measures 3386.27 m²

These figures indicate that the recommended multipliers receive a greater volume of direct messages (DMs) than any other comparable multiplier. Consequently, for image processing tasks constrained by space or power, the recommended multipliers are the optimal choice.

## APPLICATION OF PROPOSED MULTIPLIER

This section will illustrate the application of the proposed criteria to various image processing tasks. Enhancing and expanding images are two instances of image processing techniques that frequently employ image multiplication. This paper is evaluating the recommended variables for their use in conjunction with visual data. We are merging two distinct test images to produce a new image.




Fig.4. Multiplication of test images using 8×8 exact Wallacemultipliers (a) Image-1 (b) Image-2 (c) Exact Multiplication

Figures 4(a) and (b) illustrate visual verifications of the multiplication procedure. Both files exemplify the "portable network graphics" (PNG) format and each has a size of 512 bytes. The test images were selected due to their absence of essential elements for image analysis. There are a total of 262,144 images, each containing 512 pixels. The permissible values for this 8-bit unsigned number range from zero to two hundred fifty. We assembled the two test images pixel by pixel. The result of multiplying the example photographs by 88 is illustrated in Figure 4(c). By photomultiplying all alternative multiplier designs, we can evaluate their PSNR. Figure 5 has several photographs from the shoot.

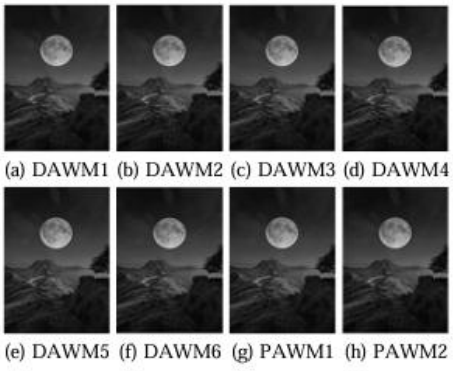



Fig.5. To multiple the test photographs, one of the 88 Wallace multipliers that were suggested and informally built was employed.

The picture quality is evaluated in MATLAB by calculating the "peak signal-to-noise ratio" (PSNR) for each multiplier, as illustrated in Fig. Section 4(c). Table 7 presents the anticipated PSNR values for each design. Table 7 indicates that PAWM1 possesses a PSNR of 51 dB, while PAWM2 exhibits a PSNR of 51.355 dB. There exist additional multipliers whose values are congruent with this one. The proposed multipliers yield superior PSNR outcomes compared to DAWM2, DAWM4, and DAWM6, although they are inferior to DAWM1, DAWM3, and DAWM5. It is widely believed that the PSNR of the next-generation PAWM1 and PAWM2 repeater designs will surpass that of current systems.

Table.7. PSNR is used to test and compare Wallace multipliers that have been created and suggested.

| AWM | PSNR (dB) |
|---|---|
| DAWM1 | 52.996 |
| DAWM2 | 50.688 |
| DAWM3 | 52.106 |
| DAWM4 | 48.744 |
| DAWM5 | 55.511 |
| DAWM6 | 47.386 |
| PAWM1 | 51.000 |
| PAWM2 | 51.355 |

## 4. CONCLUSION

We developed and evaluated the proposed Wallace multipliers PAWM1 and PAWM2 for estimation in this paper. These were utilized to evaluate the proposed multipliers against other designs and assess their efficacy. The comparison indicates that the proposed multipliers yield superior outcomes compared to the alternative multipliers regarding DMs. Alongside the image multiplication example, the proposed multipliers can provide high-quality photographs with optimal and comparable PSNR. The application of the proposed multipliers as an alternative for image processing tasks that necessitate low power consumption, compact size, and elevated PSNR is both logical and beneficial.

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